SPICE OPERATIONAL AMPLIFIER MACRO-MODEL

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Introduction

This application note describes the SPICE macro-model for the HA-2539 op amp. The model was designed to be compatible with the well known SPICE program developed by the University of California in hope that most simulation software vendors follow this basic format and syntax. A schematic of the macro-model, the SPICE net listing and various simulated performance curves are included. The macro-model schematic includes node numbers to help relate the SPICE listing to the schematic. The model simulates most AC and DC parameters. The significant dominant poles and zeros are included to give the most accurate AC simulation with minimum model complexity.

Model Description

Input Stage

The first block (1) is the input stage of the op amp. CN1, LN and LP model the parasitic inductance and capacitance of the package and bond wires. RDF, RCN and RCP model the differential and common-mode input resistances. VOF, IBN and IBP model the input offset voltage, offset current and bias currents. CN2 and CP2 model the decrease in the common-mode input impedance with frequency. Common-mode rejection is not modeled, but could be added by making VOF a dependent source controlled by the common-mode voltage.

Gain Stage

The second block (2) models differential to single-ended conversion with gain. Voltage clamps model slew rate limiting. ED is ten times the differential input voltage. RD and CD model the bandwidth of the input stage. The diodes and voltage sources clamp the output voltage of this stage thereby modeling the slew rate.

Frequency Response

The next block (3) models the small-signal open loop frequency response. GA provides a current which is (1.43mA)*V(2,0). RH and CH model the resistance and capacitance of the high impedance node. RC and CC model the compensation network.

Poles-Zeros

The fourth block (4) models two higher order parasitic poles. EP duplicates the voltage across the compensation capacitor CC.

Output Stage and Power Supply

Finally, the output block (5) models the finite output impedance of the amplifier and the parasitic elements of the bond wire inductance and package capacitance. The last block (6) represents the op amps power supply current, IPS. Current sourced or sinked out of the op amps output will not show up as an increase in the supply current.

Parameters Not Modeled:

- Temperature Effects
- Differential Voltage Restrictions
- Input Noise Voltage and Current
- Common Mode Restrictions
- Tolerances for Monte Carlo Analysis
- Common Mode Rejection Ratio
- Power Supply Range
- Power Supply Rejection Ratio

Spice Listing

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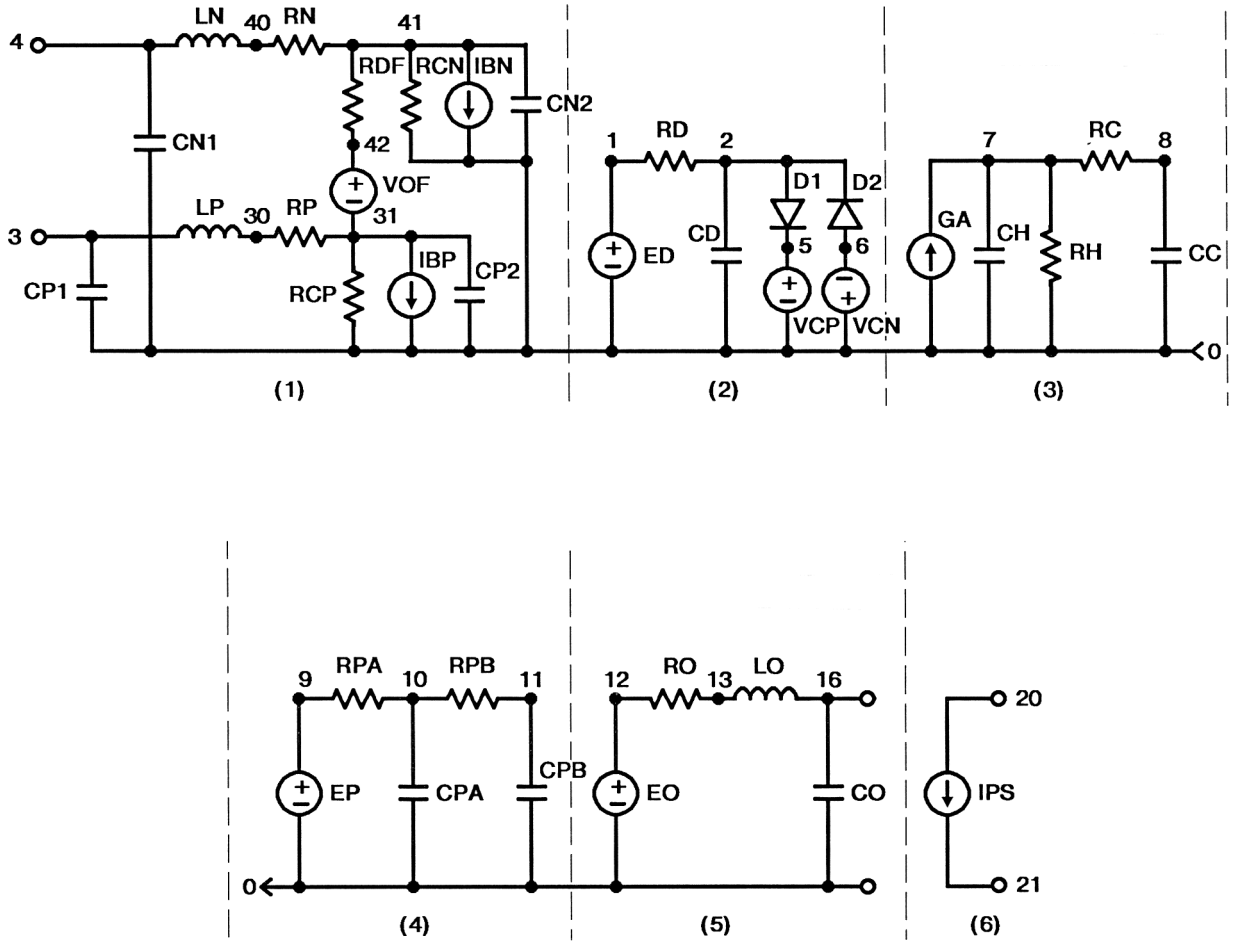
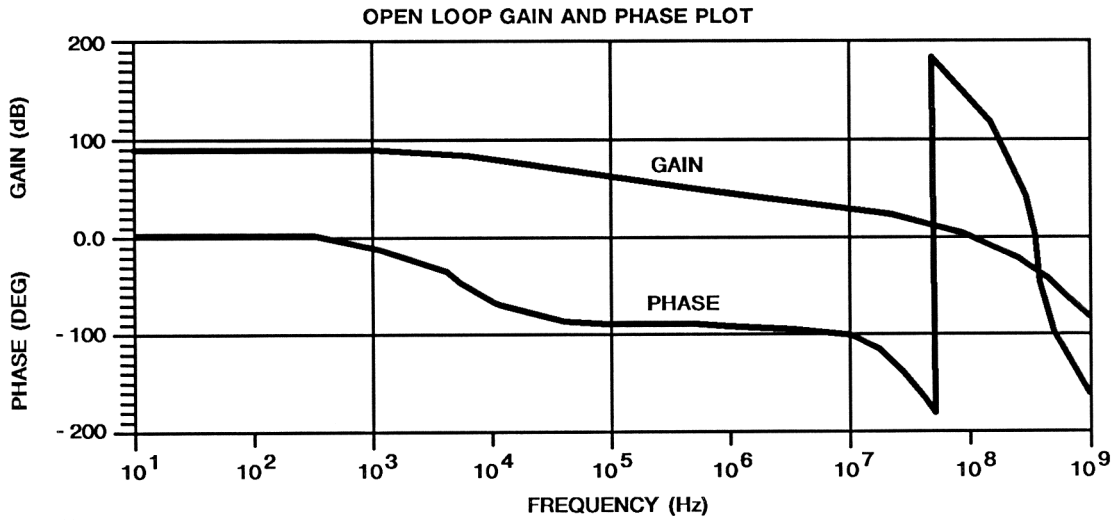
*
* HA2539 MACRO-MODEL
* REV: 8/8/91
* BY: J. COUTREAU
*
* NODE 3 -> +IN, NODE 4 -> -IN, NODE 16 -> OUTPUT
* NODE 20 -> +Vs, NODE 21 -> -Vs
*
.SUBCKT HA2539   3   4   20   21   16
*
* INPUT STAGE
*
CN1 4 0 1E-12
LN 4 40 5E-9
RN 40 41 30
RCN 41 0 10E6
IBN 41 0 10E-6
CN2 41 0 0.5E-12
CP1 3 0 1E-12
LP 3 30 5E-9
RP 30 31 30
RCP 31 0 10E6
IBP 31 0 8E-6
CP2 31 0 0.5E-12
RDF 41 42 43E3
VOF 42 31 2E-3
*
* SLEW LIMITING
*
ED 1 0 42 41 10
RDA 1 33 75
CDA 33 0 7E-12
RDB 33 2 75
CDB 2 0 3E-12
D1 2 5 DM OFF
D2 6 2 DM OFF
.MODEL DM D (IS=1E-9 BV=40 IBV=50E-6)
VCP 5 0 1.2
VCN 0 6 1.2
*
* COMPENSATION
*
GA 0 7 2 0 1.43E-3
RH 7 0 1.3E6
CH 7 0 1.5E-12
RC 7 8 600
CC 8 0 2.2E-12
*
* POLES
*
EP 9 0 8 0 1
RPA 9 10 75
CPA 10 0 7E-12
RPB 10 11 50
CPB 11 0 3E-12
*
* OUTPUT STAGE
*
EO 12 0 11 0 1
RO 12 13 25
LO 13 16 5E-9
CO 16 0 1E-12
*
* POWER SUPPLY CURRENT
*
IPS 20 21 20E-3
.ENDS HA2539
```

Macro-Model Schematic

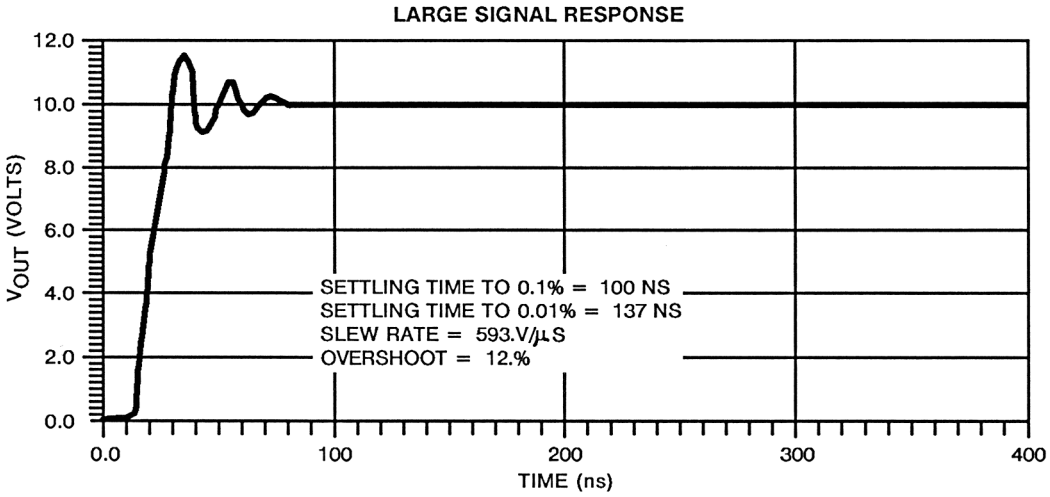


Model Performance

Conditions: V_{SS} = ±15V, A_{VCL} = +10, Unless Otherwise Specified



Model Performance (Continued)



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